REMARKS

Claims 1, 2, 5-9, 12-17, 19, 21-23, 25-31, 33-38, and 40-43 are pending. Claims 3, 4, 10, 11, 18, 20, 24, 32, and 39 have been previously cancelled. Claims 1, 5, 12, 15, 21, 26, 30, 33, 37 and 40 have been amended. No new matter has been introduced. Reexamination and reconsideration of the application are respectfully requested.

The applicant would like to thank the Examiner for setting up an interview on short notice on January 7, 2009 in order to discuss the amendment set forth in this RCE and amendment. In the August 7, 2008 Office Action, the Examiner rejected claims 5, 12, and 21 under 35 U.S.C. §103 (a) as being unpatentable over Kim, US PG Pub 2004/0093461 ("the Kim reference"), in view of U.S. Patent No. 5,761,703 to Bolyn ("the Bolyn reference"). The Examiner rejected claims 1-2, 6-9, 13-15, 23, 25-31, 33-38, and 40-43 under 35 U.S.C. §103 (a) as being unpatentable over the Kim reference in view of US Patent 6,871,261 to Proebsting ("the Proebsting reference") further in view of the Bolyn reference. The Examiner rejected claims 16-17, 19, and 22 under 35 U.S.C. §103 (a) as being unpatentable over the Kim, Proebsting, and Bolyn references as applied to claims 1-2, 6-9, 13-15, 23, 25-31, 33-38, and 40-43 above, in view of U.S. Patent No. 6,195,303 to Zheng ("the Zheng reference"). The Examiner's rejections are respectfully traversed.

Claim 1 specifies:

> A method of operating a memory device having multiple memory bank arrays and being responsive to command signals and a plurality of bank address signals, the method comprising:
> specifying at least one of a multiple of memory bank arrays to be refreshed using a plurality of bank address signals;
> initiating in response to first command signals an auto-refresh

command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays; and

initiating, before or during the auto refresh operation to the at least one of the specified memory bank arrays, a second command signal controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed, **wherein multiple rows of the at least one memory bank array is refreshed in a staggered fashion relative to other rows in the memory bank array per the auto-refresh command and the second operation begins after all the rows have begun the auto refresh operation.**

In the January 28, 2008 Office Action, the Examiner states that the Kim reference does not teach the last limitation of claim 1. *(Office Action, page 5)*. The applicant agrees with the Examiner and respectfully submits that claim 1 distinguishes over the Kim reference.

The Examiner also states that the Proebsting reference discloses the non-bolded portion of the last limitation of claim 1. Assuming, *arguendo*, that the Examiner's statements are correct regarding the Proebsting reference, the Examiner also states that the Proebsting reference does not discloses a staggered refresh. *(Office Action, page 5)*. The Applicant also agrees with the Examiner regarding the Proebsting reference not disclosing the staggered refresh. Accordingly, applicant respectfully submits that claim 1, as amended, distinguishes over the Proebsting / Kim combination.

The Bolyn reference does not make up for the deficiencies of the Proebsting and Kim references. The Examiner states that the Bolyn reference discloses a staggered refresh wherein multiple rows per memory bank are refreshed in a staggered fashion. *(Office Action, page 5)*. The applicant amended the independent claims to identify that multiple rows of at the at least one memory bank array are refreshed in a staggered

fashion relative to other rows in the memory bank array to further clarify the invention.

The Bolyn reference discloses a value of a refresh time spread out over a number of rows in each DRAM segment and the number of segments that are supported by the memory board. This technique allows the Bolyn reference to stagger DRAM module refreshes. *(Bolyn, col. 5, lines 29 – 33).* This is not the same as **wherein multiple rows of the at least one memory bank array are refreshed in a staggered fashion relative to other rows in the memory bank array per the auto-refresh command**, as is recited in claim 1, as amended. It is not the same because the Bolyn reference is referring to staggering the refreshes of DRAM modules, i.e., to stagger the module 1 refresh as compared to the module 2 refresh as compared to the module 3 refresh. There is no disclosure in the Bolyn reference that multiple rows of the at least one memory bank array are refreshed in a staggered fashion relative to other rows in the at least one memory bank array, as is recited in claim 1, only that the DRAM module refreshes are staggered. Accordingly, applicant respectfully submits that claim 1, as amended, distinguishes over the Kim / Proebsting / Bolyn combination.

Independent claims 5, 12, 26, 30, 33, 37 and 40, all as amended, recite limitations similar to claim 1 as amended. Accordingly, applicant respectfully submits that claims 5, 12 ,26, 30, 33, 37 and 40 distinguish over the Kim / Proebsting / Bolyn combination for reasons similar to those discussed above in regard to claim 1.

Claims 2, 6 – 9, 13, 14, 27 – 29, 21, 34 – 36, 38 and 41 – 43 depend, directly or indirectly, on independent claims 5, 12, 26, 30, 33, 37 and 40. Accordingly, applicant respectfully submits that claims 2, 6 – 9, 13, 14, 27 – 29, 21, 34 – 36, 38 and 41 – 43 distinguish over the Kim / Proebsting / Bolyn combination for the same reasons as

those discussed above in regard to claim 1.

Independent claims 15 and 21, recite similar limitations to claim 1. Independent claims 15 and 21 were further rejected under the Zheng reference. The Examiner states that the Zheng reference teaches an order of refreshing, i.e., wherein the at least one specified memory bank array of the multiple memory bank arrays is determined based on which memory bank arrays have been refreshed and a subsequent known order of refreshing the memory bank arrays. *(Office Action, page 17)*. Assuming, *arguendo*, that the Zheng reference discloses all that the Examiner states that it does, the Zheng reference does not disclose **wherein multiple rows of the at least one memory bank array are refreshed in a staggered fashion relative to other rows in the memory bank array per the auto-refresh command**, as is recited in claims 15 and 21. Accordingly, applicant respectfully submits that claims 15 and 21 distinguish over the Zheng / Kim / Proebsting / Bolyn combination.

Claims 16, 17, 19, 22, 23 and 25 depend, directly or indirectly, on claims 15 and 21. Accordingly, applicant respectfully submits that claims 16, 17, 19, 22, 23 and 25 distinguish over the Zheng / Kim / Proebsting / Bolyn combination for the same reasons as those discussed above in regard to claims 15 and 21.

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Applicant believes that the foregoing remarks place the application in condition for allowance, and a favorable action is respectfully requested. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles telephone number (213) 488-7100 to discuss the steps necessary for placing the application in condition for allowance should the examiner believe that such a telephone conference would advance prosecution of the application.

Respectfully submitted,

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